ABSTRACT OF THE DISCLOSURE

A semiconductor integrated circuit is disclosed, in which a memory is activated at high speed in commensurate with a high-speed logic circuit mounted with the memory in order to reduce the cost using a DRAM of a 3-transistor cell requiring no capacitor. A pair of data lines connected with a plurality of memory cells having the amplification function are set to different precharge voltage values, thereby eliminating the need of a dummy cell. The elimination of the need of the dummy cell unlike in the conventional DRAM circuit using a gain cell reduces both the required space and the production cost. A hierarchical structure of the data lines makes a high-speed operation possible. Also, a DRAM circuit can be fabricated through a fabrication process matched with an ordinary logic element.